CONTINUOUS INTERNAL EVALUATION- 3

Dept:ECE	Sem / Div:5 ECE	Sub:Verilog HDL	S Code:18EC56
Date: 15-01-2021	Time:2:30 - 4:00PM	Max Marks: 50	Elective:N

Note: Answer any 2 full questions, choosing one full question from each part.

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QN		Questions	Marks	RB	COs
		PART A			
1	a	Bring out the difference between task and functions	8	L3	CO4
	b	Write a verilog program to call a function called calc_parity which computes the parity of a 32 bit data,[31-0] data and display odd or even parity message.	8	L3	CO4
	c	What is parameter overriding and why it is needed? Discuss different techniques of parameter overriding with an example for each	9	L2	CO4
		OR			
2	a	Explain force and release statement with an example.How is it different from assign.	9	L2	CO4
	b	Discuss the system tasks related to files	6	L2	CO4
	c	With a neat flow chart explain computer aided logic synthesis process.	10	L2	CO4
		PART B			
3	a	Define the term logic synthesis.	5	L2	CO4

	b	What will the following statement translate to when run on a logic synthesis tool.
		i. assign y=(a&b)| (c & d) where out,a,b,c,d are 3 bit vectors
		ii. if(s)
		out=i1;
		else
		out=i0;
			10	L2	CO4

	c	With a neat flow chart explain logic synthesis flow from RTL to Gates	10	L2	CO4
		OR			
4	a	With a example program explain conditional compilation and conditional execution.	12	L3	CO4
	b	With a example explain the use of input and output arguments in tasks.	8	L3	CO4
	c	Explain the syntax of task declaration and invocation.	5	L2	CO4

Jovita

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HOD